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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,729	11/06/2001	Takayuki Shinkawa	0941.65970	1120

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Patrick G. Burns, Esq.
GREER, BURNS & CRAIN, LTD.
Suite 2500
300 South Wacker Dr.
Chicago, IL 60606

EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,729	SHINKAWA ET AL.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *4-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 9-11* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *November 6, 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are presented for examination. A restriction was mailed to the applicant on December 4, 2003 as paper number 4. Group I was elected with traverse. Claims 1-3 and 9-13 will be examined and claims 4-8 are withdrawn from consideration. The restriction given in paper #4 is hereby repeated below.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-3 and 9-13, drawn to regulating buffer access, classified in class 711, subclass 151.

II. Claims 4-8, drawn to memory testing, classified in class 714, subclass 718.

3. The inventions are distinct, each from the other because: claims 1-3 and 9-13 are directed to memory accesses involving different memories, a control unit and a buffer manager while claims 4-8 are specifically directed to testing in relationship to an internal logic circuit using a test register.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Applicant's election with traverse of the restriction of claims 1-3 and 10-13 as group I and claims 4-8 as group II in Paper No. 4 is acknowledged. The traversal is on the ground(s) that 'the elected and non-elected claims share various features in common, so a search for the elected group would likely overlap with a search for the non-elected group'. This is not found

persuasive because the claims of the elected group is best classified in a different class than the claims of the non-elected group.

5. The requirement is still deemed proper and is therefore made FINAL.

Drawings

6. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

9. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

11. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozakai et al.

12. Kozakai teaches the invention (claim 1) as claimed including a data processing device in which a processor processes data based on a stored program and a buffer manager accesses the data with the buffer manager taught as a microcomputer positioned on a memory card which controls the memory card including the different buffers and memories (e.g., see Figure 1), the data processing device comprising:

a program memory storing program codes, the program codes being loaded into the program memory and executed by the processor when processing the data with the memory card included in a system through the interface and control logic circuit (e.g., see Figure 1 and col. 4, line 34 to col. 5, line 5 and Figure 5 and col. 7, lines 5-39);

a shared memory storing one of the program codes and the data is taught as flash memory which stores both program codes and data or the shared memory could be interpreted as a main memory for an overall system which is shown as a host apparatus (e.g., see Figures 1-3); and,

a control unit selectively connecting the processor and the buffer manager to the shared memory based on a select pattern, wherein the shared memory functions to store the program codes when the select pattern is set in a first condition and the shared memory functions to store data when the select pattern is set in a second condition, this functionality is taught as the buffer RAM, element 7 of Figure 1, being used as an extended program memory with a vector table having a VCT1, VCT2 or VCT3 containing information indicative of the extended program memory (e.g., see Figure 5 and col. 7, lines 5-39). Additionally, the flash memory can be used for either data or programs with using the mode control circuit to discriminate between commands (program code), data or addresses (e.g., see Figure 16 and col. 11, lines 6-19) also teaches the actual claim language.

As to claim 2, Kozakai teaches the control unit comprises a register and a multiplexer with the select pattern being input to the register and the multiplexer selectively connecting a first connecting line and a second connecting line to the shared memory in response to the select pattern input to the register (e.g., see Figure 4).

As to claim 3, Kozakai teaches the stored program includes a large amount of program codes exceeding a storage capacity of the program memory, both the program memory and the shared memory function to store the program codes and the externally attached buffer memory is used to store the data and when the stored program includes a small amount of program codes, only the program memory functions to store the program codes and the shared memory functions to store the data as the capability of the system having a plurality of LSI memory cards with the memory cards being used either to store program codes or data as required for a particular use of the overall computer system (e.g., see Figures 2-3 and 6-12).

35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 9-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Kozakai et al.

15. Kozakai teaches the invention (claim 9) as claimed including an interface device which performs data input/output operations through a plurality of channels, the interface device comprising:

a plurality of buffer memories including a first memory buffer and a second memory buffer, each buffer memory provided for a particular channel as the ability to use a plurality of memory cards with each memory card connected to a bus or channel (e.g., see Figures 2-3); and,

a control unit controlling the data input/output operations for each of the plurality of buffer memories such that data stored in the first buffer memory and data stored in the second buffer memory are set to be identical to each other by performing data transfer between the first buffer memory and the second buffer memory is not specifically taught, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a first buffer memory contain the identical data to the second buffer memory with the second buffer memory being a backup of the first buffer memory or as an archive of the first buffer memory because this provides protection for data which has been specifically stored to a memory card using the connectivity shown in either Figure 2 or 3. This is particularly useful for a system smaller than an actual RAID type system which uses a plurality of redundant disks to achieve the same result of secure data.

As to claim 10, Kozakai teaches the control unit comprises a data management table which provides correlations between locations of respective data stored in the plurality of buffer memories and locations of data stored in a recording medium, the respective states of the stored data in the plurality of buffer memories being managed by the control unit (e.g., see col. 5, lines 6-25).

As to claim 11, Kozakai teaches the stored data of one of the buffer memories is updated through one of the channels, the control unit set the state of another channel in an access-disable state by using the data management table, thereby inhibiting receiving a command at the interface device via another channel is inherently taught as either using a memory card at a

particular port of the host apparatus or not. Each memory card provides a card select signal as an input to the host interface.

16. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (703) 305-9706. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (703) 308-1756. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center receptionist whose telephone number is (703) 305-3800/4700.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

February 11, 2004